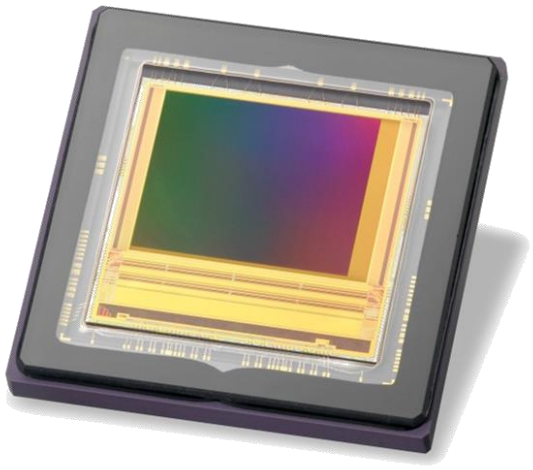
EV76C664 Datasheet
1.3 Mpixels Monochrome and Sparse CMOS Image sensor

FEATURES

- 1.3 million (1280 x 1024) pixels, 10 µm square pixels with shifted micro-lens
- Optical format 1”
- Aspect Ratio : 5/4
- 100fps @ full resolution & 12bit / 60fps @ full resolution & 12bit & DDS
- Output format true 8 / 10 / 12 / 14bit LVDS and synchronization
- SPI controls
- Control input pins: Trigger In, Reset
- Light control output – Trigger out
- 3.3 V and 1.8 V power supplies
- 80 MHz input clock
- 67 pins PGA ceramic package
- Anti-Reflective window



Embedded functions:

- Image Statistics and Context output
- Sub-sampling (Horizontal / Vertical)
- Two PLL for LVDS and ADC frequencies generation
- Wide Dynamic Range capabilities
- Accumulation mode for active imaging applications
- Time to Read improvement (good first image, abort image)

Timing modes:

- Global shutter in Serial and Overlap modes
- Global Shutter with external CDS mode
- Rolling shutter in Serial and Overlap modes

PERFORMANCE CHARACTERISTICS

- High sensitivity at low light level
- Operating temperature [-30° to +65°C]
- Peak QE > 66%

AVAILABLE SENSOR TYPES

- Monochrome
- Sparse Color Filter Array

APPLICATIONS

- Surveillance & Security cameras
- Traffic cameras
- Industrial inspection
- Biometric and Medical imaging
- Military and Law Enforcement
- Scientific imaging / Astronomy

INTRODUCTION

The EV76C664 is a 1.3 million pixels CMOS image sensor, designed with e2v's proprietary CMOS imaging technology. It is ideal for many different types of application where superior performance is required. The innovative pixel design offers excellent performance in low-light conditions with an electronic global shutter (true snapshot), and offers a high-readout speed at 100 fps in full resolution and 12bit.

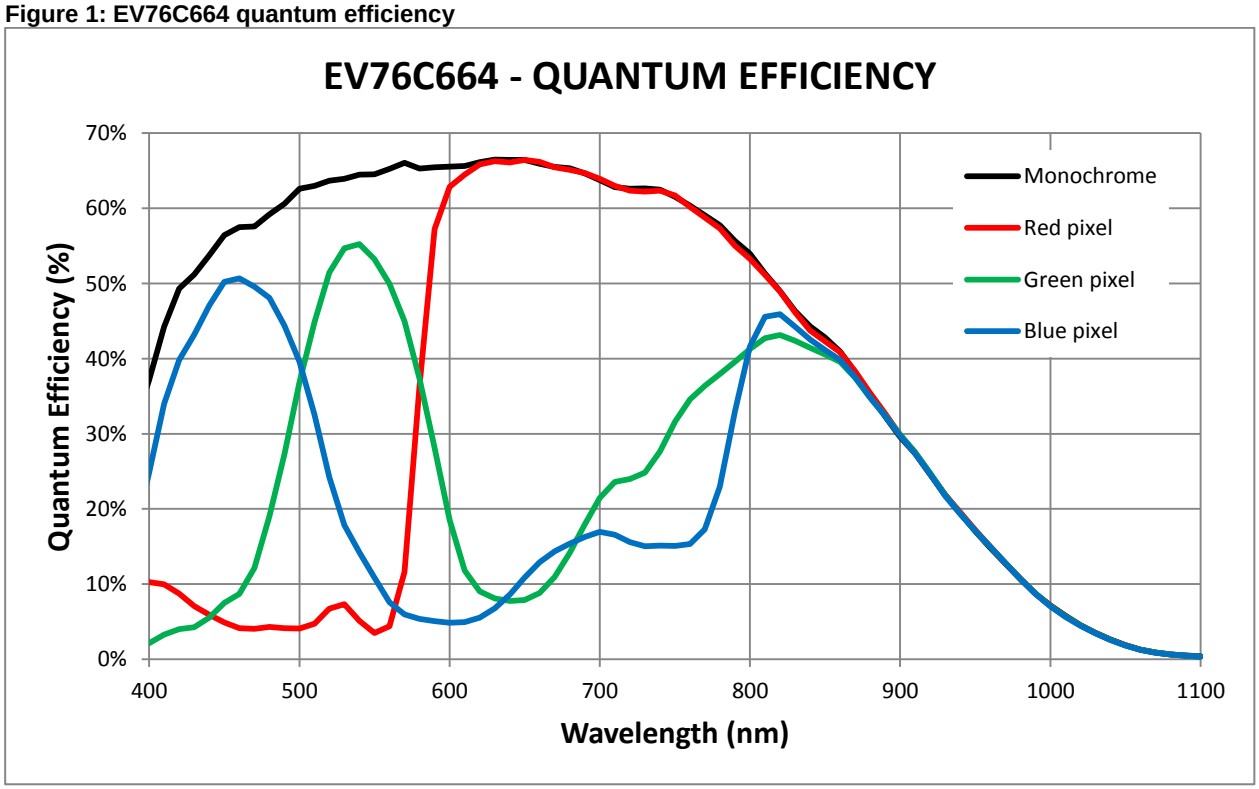
1. TYPICAL PERFORMANCE DATA

Table 1: Typical electro-optical performances @ 25°C and 70°C ambient temperatures, nominal pixel clock (80MHz)

Parameter		Unit	Typical Value	
Sensor characteristics	Resolution	pixels	1280 (H) x 1024 (V)	
	Image size	mm inche	12.8 (H) x 10.2 (V) – 16.4 (diagonal) 1	
	Pixel size (square)	µm²	10 x 10	
	Aspect ratio		5/4	
	Max frame rate[6]	fps	210 @ full resolution & 8bit 180 @ full resolution & 10bit 100 @ full resolution & 12bit 30 @ full resolution & 14bit	
	Pixel rate	Mpixels / s	131 maximum @12bit	
	Bit depth	bit	8 – 10 – 12 - 14	
Pixel performance			@ T_A 25°C	@ T_A 70°C
	Dynamic range	dB	> 67 [1b] / > 73 [1a]	"
	Qsat / SNR max	ke- / dB	14 / 41	"
	Readout Noise	e- (GS/DDS/ERS)	18 / 6 / < 3	
	MTF at Nyquist, λ=550 nm	%	67	
	Dark signal[2]	LSB_{12}/s	2	1000
	DSNU[2]	LSB_{12}/s	10	160
	PRNU [3] (RMS)	%	< 1	
	Responsivity [4]	LSB_{12}/(µJ/cm²)	450 000	
Electrical interface	Power supplies	V	3.3 & 1.8	
	Power consumption : Functional[5] Standby	mW mW	< 400 < 2	

(1a): in electronic rolling shutter (ERS) mode
(1b): in global shutter digital double sampling (DDS) mode
(2): min gain, 12bit
(3): measured @ Vsat/2, min gain
(4): min gain, 550nm, window with AR coating
(5): @ 100fps & full format & with 10 pF on each output
(6): in single ADC mode

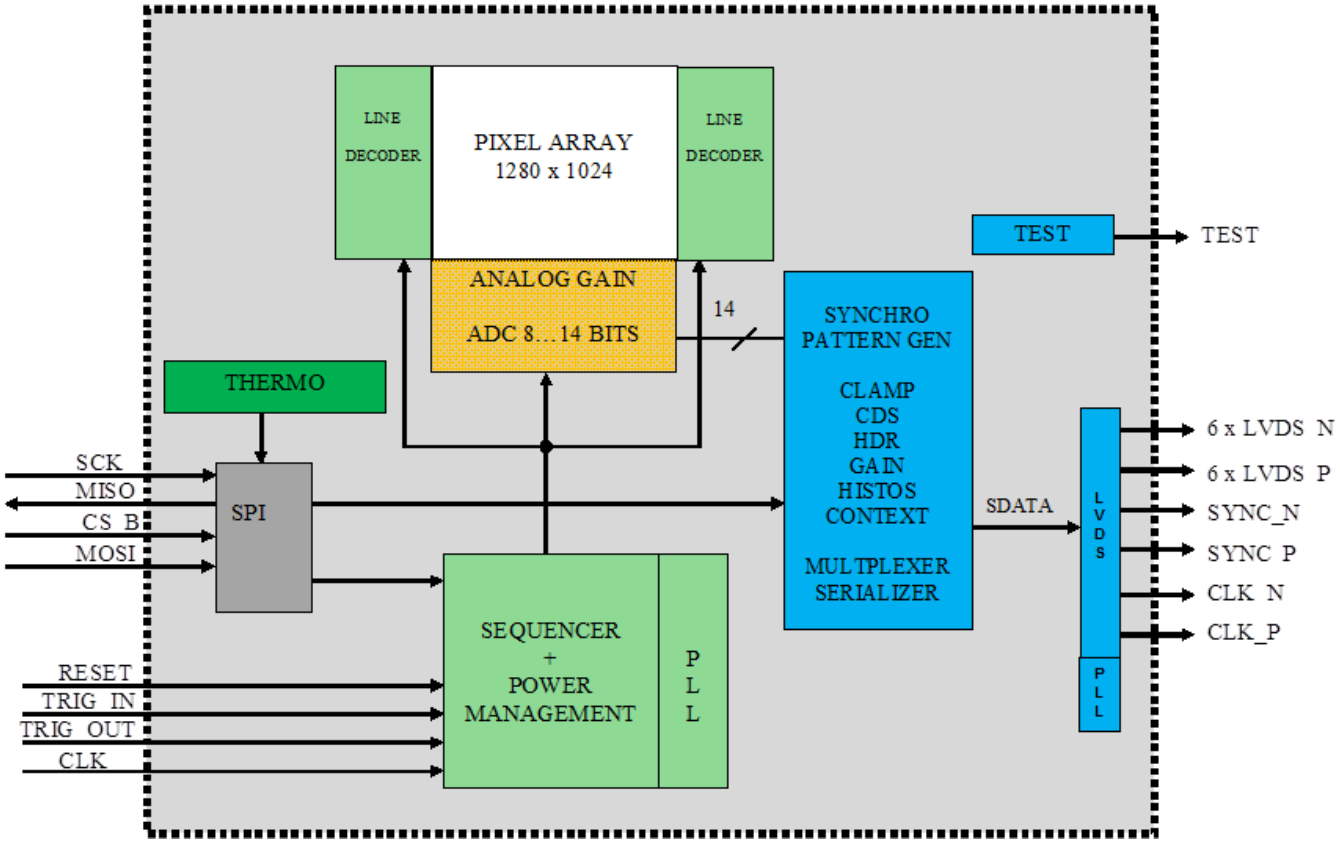
Figure 1: EV76C664 quantum efficiency



2. SENSOR OVERVIEW

The EV76C664 image sensor active area is 1408 x 1040 pixels and the useful pixel area is 1280 x 1024 pixels.

Figure 2: Block diagram



3. APPLICATION INFORMATION

This paragraph gives the top view pinout, the pin list and the power supplies decoupling.

Figure 3: Pinout Top View

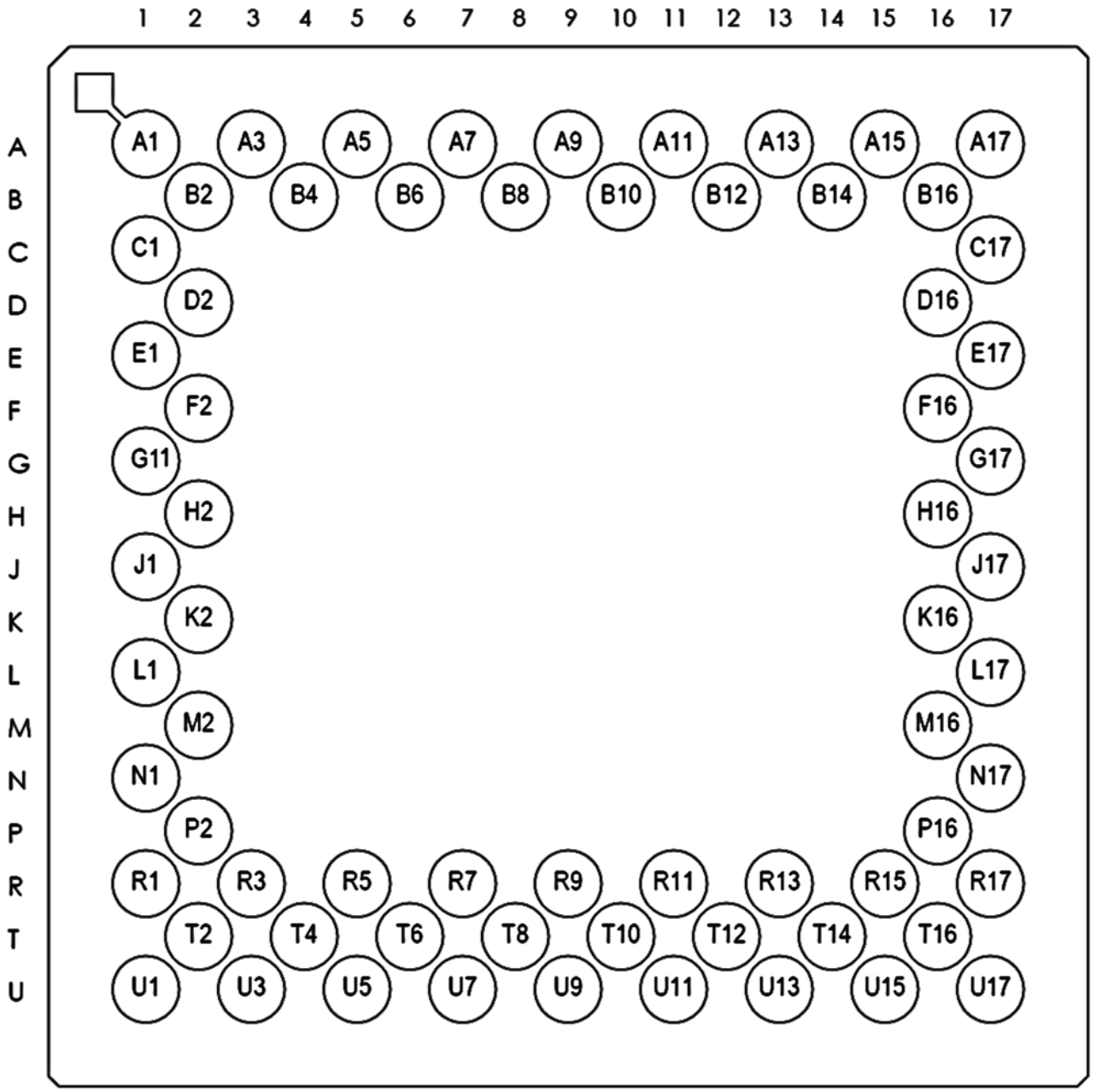


Table 2 : Pinout Table

Pin Number	Pin Number	Name	Type	Electrical level
1	A1	VDD33A	Analog power supply	3.3V
2	A3	VDD_MAT	Analog power supply	
3	A5	VDD_DL	Analog power supply	
4	A7	NC		
5	A9	VHR_MEM	(optional external power supply)	
6	A11	NC		
7	A13	VNEG (NC)	Analog power supply	
8	A15	VDD_DL	Analog power supply	3.3V
9	A17	VDD33A	Analog power supply	3.3V
10	B2	VSS33A	Analog Ground	Ground
11	B4	VSS_MAT	Analog Ground	Ground
12	B6	NC	Analog Test pin	
13	B8	VLR_MEM	(optional external power supply)	
14	B10	VLR_PH	(optional external power supply)	
15	B12	NC		
16	B14	VD_SF (NC)	Analog power supply	
17	B16	VSS33A	Analog Ground	Ground
18	C1	VDD33A	Analog power supply	3.3V
19	C17	VDD33A	Analog power supply	3.3V
20	D2	VSS33A	Analog Ground	Ground
21	D16	VSS33A	Analog Ground	Ground
22	E1	VDD18A	Analog power supply	1.8V
23	E17	VDD18A	Analog power supply	1.8V
24	F2	VSS18A	Analog Ground	Ground
25	F16	VSS18A	Analog Ground	Ground
26	G1	VDD18A	Analog power supply	1.8V
27	G17	VDD18A	Analog power supply	1.8V
28	H2	VSS18A	Analog Ground	Ground
29	H16	VSS18A	Analog Ground	Ground
30	J1	NC		
31	J17	NC		
32	K2	SCAN_MODE	Digital test pin	VDDIO
33	K16	NC		VDDIO
34	L1	TRIG_OUT	Trigger Out	VDDIO
35	L17	CS_N	Chip Select	VDDIO
36	M2	RESET_N	SPI Reset	VDDIO
37	M16	SCK	SPI Clock	VDDIO
38	N1	TRIG_IN	Trigger In	VDDIO
39	N17	MISO	SPI MISO	VDDIO
40	P2	CLK_EXT	Input Clock	VDDIO
41	P16	MOSI	SPI MOSI	VDDIO
42	R1	VSS1833D	Digital Ground	Ground
43	R3	VSS18A	Analog Ground	Ground
44	R5	VDD18A	Analog power supply	1.8V
45	R7	VDD33D	Digital power supply	3.3V
46	R9	VSS1833D	Digital Ground	Ground
47	R11	VDD18D	Digital power supply	1.8V
48	R13	VDD18A	Analog power supply	1.8V
49	R15	VSS18A	Analog Ground	Ground
50	R17	VSS1833D	Digital Ground	Ground

Pin Number	Pin Number	Name	Type	Electrical level
51	T2	N_LVDS0	Negative LVDS data 0	LVDS
52	T4	N_LVDS1	Negative LVDS data 1	LVDS
53	T6	N_LVDS2	Negative LVDS data 2	LVDS
54	T8	N_LVDS_CLK	Negative LVDS Clock	LVDS
55	T10	N_LVDS_CTRL	Negative LVDS Control	LVDS
56	T12	N_LVDS3	Negative LVDS data 3	LVDS
57	T14	N_LVDS4	Negative LVDS data 4	LVDS
58	T16	N_LVDS5	Negative LVDS data 5	LVDS
59	U1	P_LVDS0	Positive LVDS data 0	LVDS
60	U3	P_LVDS1	Positive LVDS data 1	LVDS
61	U5	P_LVDS2	Positive LVDS data 2	LVDS
62	U7	P_LVDS_CLK	Positive LVDS Clock	LVDS
63	U9	P_LVDS_CTRL	Positive LVDS Control	LVDS
64	U11	P_LVDS3	Positive LVDS data 3	LVDS
65	U13	P_LVDS4	Positive LVDS data 4	LVDS
66	U15	P_LVDS5	Positive LVDS data 5	LVDS
67	U17	VDD_IO	IO Power Supply	1.8V – 3.3V

NC stands for **Not Connected**.
Note: **VDDIO** is used for all **SPI**, **TRIG IN/OUT**, **RESETN** and **CLK_EXT** pins

Table 3 : Power Supply Decoupling

Pins	Name	Decoupling (per pin)	Power Consumption	Comments
A5, A15	**VDD_DL** (1)	20µF / 100nF (optional)	0 150mA peak	- Left floating by defaut (internal regulator) - // 100nF if external regulator
A3	**VDD_MAT** (1)	10µF / 100nF (optional)	12mA 250mA peak	- Left floating by defaut (internal regulator) - // 100nF if external regulator
E1, E17, G1, G17, R5, R13	**VDD18A**	1µF // 100nF	16mA 50mA peak	Analog 1,8 V (PLL, ADC)
R11	**VDD18D**	1µF // 100nF	300mA 800mA peak	Digital 1,8V (RAM, ...)
A1, A17, C1, C17	**VDD33A**	1µF // 100nF	300 mA 400mA Peak	ADC and Internal regulators
R7	**VDD33D**	1µF // 100nF	75mA 90mA	LVDS output
U17	**VDDIO**	1µF // 100nF	1mA	to be connected to FPGA outputs (1.8V to 3.3V)
A9	**VHR_MEM**	100nF (optional)		- Left floating by defaut - // 100nF if external regulator
B8	**VLR_MEM**	100nF (optional)		- Left floating by defaut - // 100nF if external regulator
B10	**VLR_PH**	100nF (optional)		- Left floating by defaut - // 100nF if external regulator
B2, B16, D2, D16, F2, F16, H2, H16, R3, R15	**VSS_18_33A**			Analog Ground
R1, R9, R17	**VSS_18_33D**			Digital Ground

(1) Optional: VDD_DL and VDD_MAT are used if external power supply is needed.

Note 1: **VDDIO** is used for all **SPI**, **TRIG IN/OUT**, **RESETN** and **CLK_EXT** pins
Note 2: It is recommended to use X7R for all the 100nF capacitors.

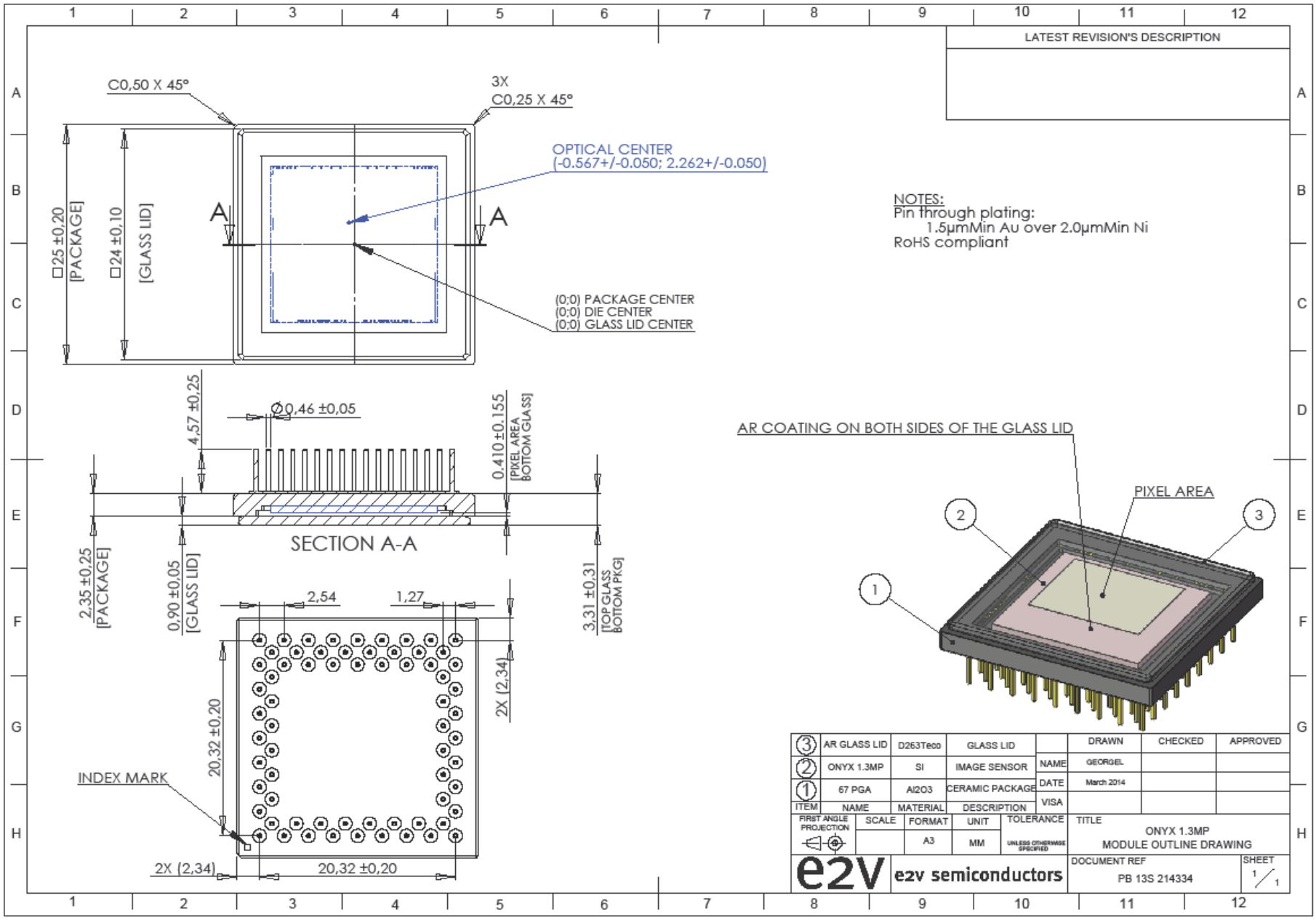
4. PACKAGE SPECIFICATION

This paragraph gives the package drawing and the window characteristics.

Table 4 : Window Characteristics

Parameters	Specification
Window material	SCHOTT D263 EcoT
Window thickness	0.9 +/-0.05 mm
Window index	ne = 1.5255
AR Coating Transmittance (400-900nm)	> 97%

Figure 4 : PGA 67 Pins Package Drawing



5. SENSOR OPERATING STATES

The sensor has different operating states as described below.

5.1 Stand By state

The Stand By state is the lowest power consumption state. The SPI registers can be programmed during the Stand By state.

5.2 Idle state

The Idle state is equivalent to a “break” mode where the sensor is waiting for a trigger. The power consumption is low but the sensor is still active.

5.3 Free Run state

In the “Free Run” mode, the sensor output frames without any user’s action. The frame rate is controlled by the integration time, the waiting time, specific functions and/or the clocks supplied to the sensor.

5.4 Trigger state

The sensor can be triggered using an external signal and/or by SPI registers. A single pulse launches an acquisition composed by consecutive integration time + readout time + optional wait time. A continuous trigger signal is equivalent to the free run mode. The sensor also provides a “pipelined” trigger mode for frame rate improvement, and an Integration Time Control (exposure controlled by the trigger).

6. READOUT MODES DESCRIPTION

The sensor offers several readout modes:

- Global Shutter
- Electronic Rolling Shutter
- Digital Double Sampling (in Global Shutter)
- Serial / Overlap modes
- Video mode

6.1 Electronic Rolling Shutter mode (ERS)

The Electronic Rolling Shutter mode allows integration and readout line by line. The ERS introduces readout distortion, but the readout noise is as low as possible.

6.2 Global Shutter mode (GS)

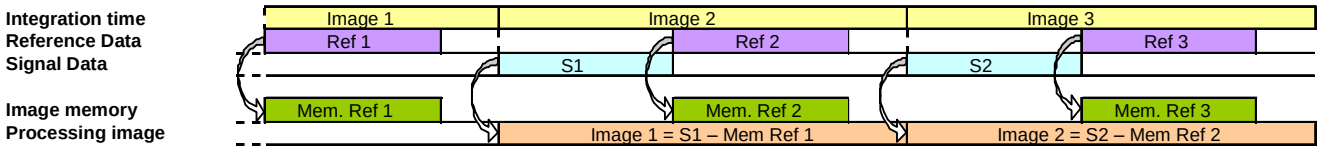
The Global Shutter mode allows true snapshot readout. The GS does not introduce any distortion during the integration and readout. The readout noise is higher compared to the ERS mode (except if DDS mode is used; see below).

6.3 Digital Double Sampling (DDS)

The Digital Double Sampling (DDS) is a function similar to the Correlated Double Sampling (CDS) but done in the digital domain (after the signal is converted by the ADC) rather than in the analog main (before the ADC). It allows a readout noise reduction especially when the Global Shutter mode is used.

The sensor outputs 2 consecutive images: a first image with the all the pixel reference levels followed by an image with all the pixel signal levels. Subtraction product of these two images will generate a low readout noise global shutter image. An off-chip image processing with external memory will be required to perform this subtraction.

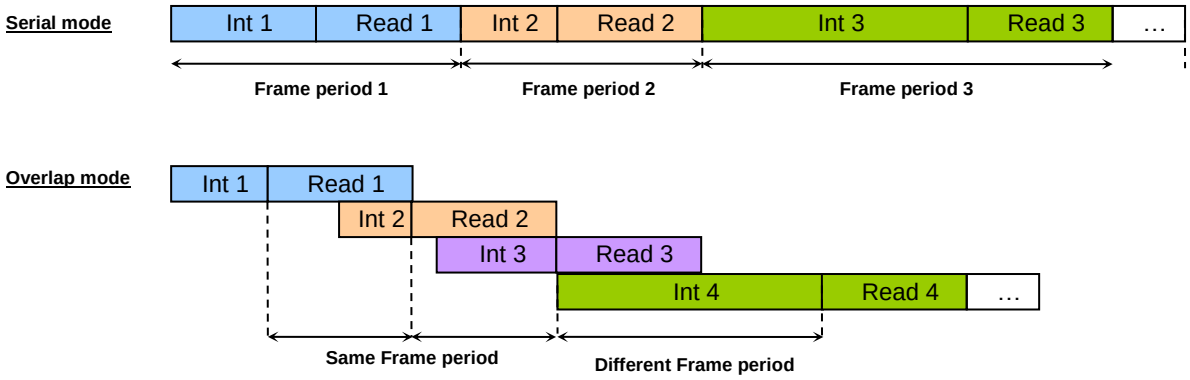
Figure 5 : Digital Double Sampling timing



6.4 Serial and Overlap mode

A sensor acquisition is composed of an integration time followed by a readout time. When the sensor is in free run mode or in video mode, there are 2 ways to output images:
- The **Serial mode** outputs each acquisition one after the other. The frame rate in this case is dependent on the integration time and readout time (ROI size).
- The **Overlap mode** allows the overlapping of readout time and integration time. In this mode, the highest frame rate can be achieved. Frame rate remains at maximum while the integration time is lower than the readout time.

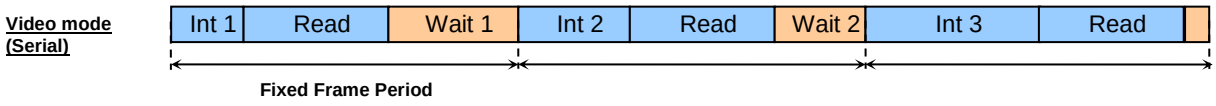
Figure 6 : Overlap and Serial modes



6.5 Video mode

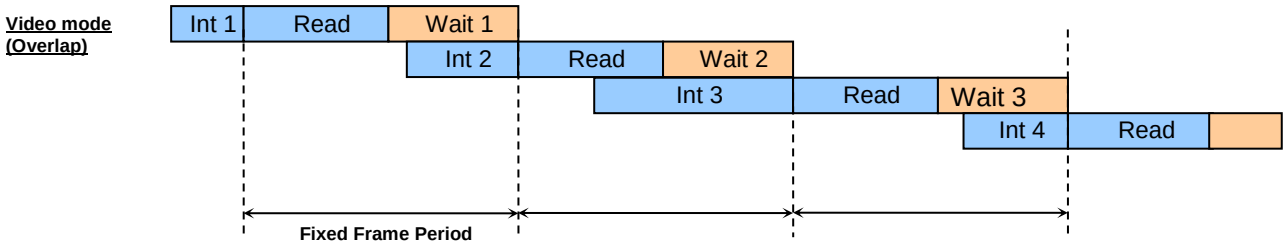
In Video mode, the frame rate is fixed and programmed through dedicated registers. In this mode, the “wait time” between frames is calculated automatically, based on the integration and readout times (**Int** and **Read** in figures below).

Figure 7 : Video mode in Serial



In serial mode, the really first frame is always in serial mode.

Figure 8 : Video mode in Overlap



7. ON-CHIP FUNCTIONS DESCRIPTION

The EV76C664 sensor has several on-chip analog and digital features for user convenience or to achieve higher performances.

7.1 Flip

The readout can be flipped in vertical (row flip), through SPI register programming. The horizontal flip can be achieved during the external image reconstruction. This allows easy system integration, depending on lens and optics.

7.2 Region Of Interest

The Region Of Interest (ROI) feature controls the number of columns and rows in a given frame. This operation is performed after the image flip but before sub-sampling and defect correction. Reducing the number of lines of the ROI increases the frame rate. The sensor can't output an odd number of rows.

7.3 Sub sampling

The sub sampling allows faster sensor readout by sampling, in horizontal and vertical, 1 pixel over 2, 4 or 8. The interest is that the field of view is fully preserved.

7.4 Trigger Out

The "Trig Out" pin outputs the exposure period used in the sensor.

7.5 Trigger In

The "Trig In" pin is used to trigger the sensor. When triggered, the sensor launches acquisition sequence.

7.6 Integration Time Control (ITC)

The ITC mode uses the Trig In to launch an acquisition with the integration time corresponding to active level of the input signal.

7.7 Output Patterns

Output patterns are digitally generated, to test the acquisition system. They can be also configured using the registers.

7.8 Analog To Digital Converter (ADC)

The Analog to Digital Converter can convert 2 rows (4 rows as an option) at a time, in true 8bit, 10bit, 12bit or 14bit.

7.9 Clock tree

The input clock is 80MHZ, by default. This clock will be directly used for internal propose and by the two internal PLLs, dedicated to LVDS and sequencer.

7.10 Wide Dynamic Range functions

The sensor offers 2 different Wide Dynamic Range modes: Logarithmic and Bi-Exposure.

7.10.1 Logarithmic

This mode sets the sensor in logarithmic response. Depending on the logarithmic adjustment, the dynamic range can reach up to 120dB.

7.10.2 Bi-Exposure

The sensor proceeds to two consecutive exposure times. The signal from each exposure is computed in the pixel to achieve a wide dynamic range image with a single readout. The ratio between the two exposures will define the extra dynamic range.

7.11 Accumulation mode

The accumulation mode allows during a global exposure time a succession of micro-integration (gated time) in the pixel. Each signal coming from a micro-integration is accumulated in the pixel memory until the pixel readout. This accumulation mode can be used in Active imaging applications like Range Gating or 3D.

7.12 Context

The Context provides additional information on sensor state. It is composed of a “Header”, output before the data, and a “Footer” output after the data.

7.13 Temperature Sensor

The EV76C664 contains one embedded temperature sensor. The temperature reading is accessible through dedicated SPI registers or through analog outputs. The temperature range is [-40°c; +85°C] and a digital calibration will be needed.

8. INTERFACE DESCRIPTION

8.1 LVDS output

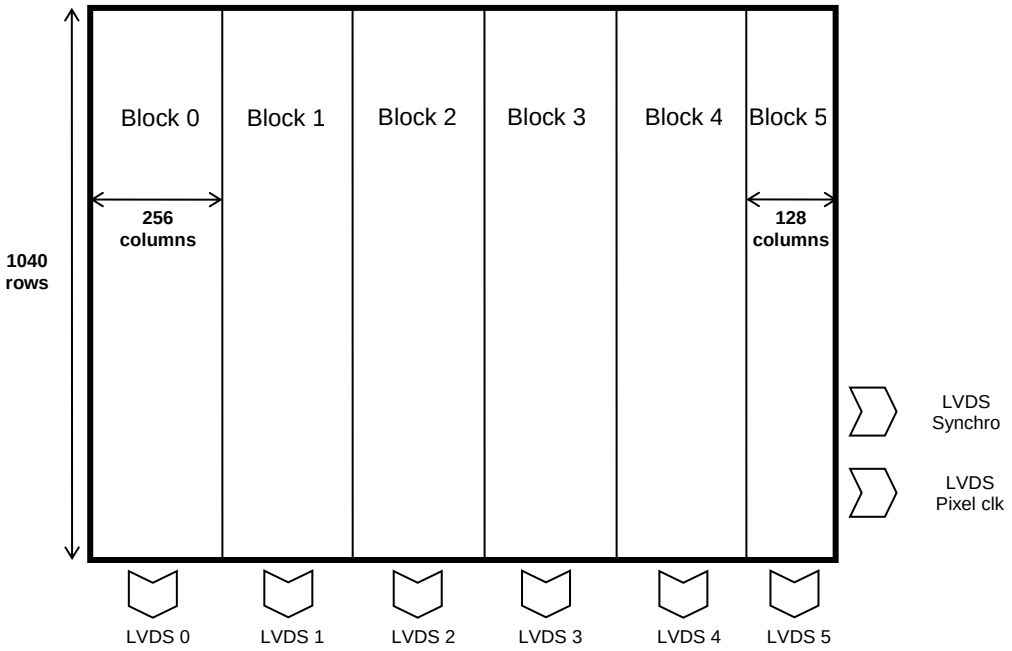
The pixel matrix is divided in 6 blocks: 5 blocks of 256 columns by 1040 rows, and 1 block of 128 columns by 1040 rows. A LVDS pair is dedicated to each block for Data output. The LVDS output voltage is:

- Standard: common voltage @ 1.2V with 350mV differential level,
- Sub-LVDS: common voltage @ 0.9V with 175mV differential level.

The 8 LVDS pairs are arranged as below:

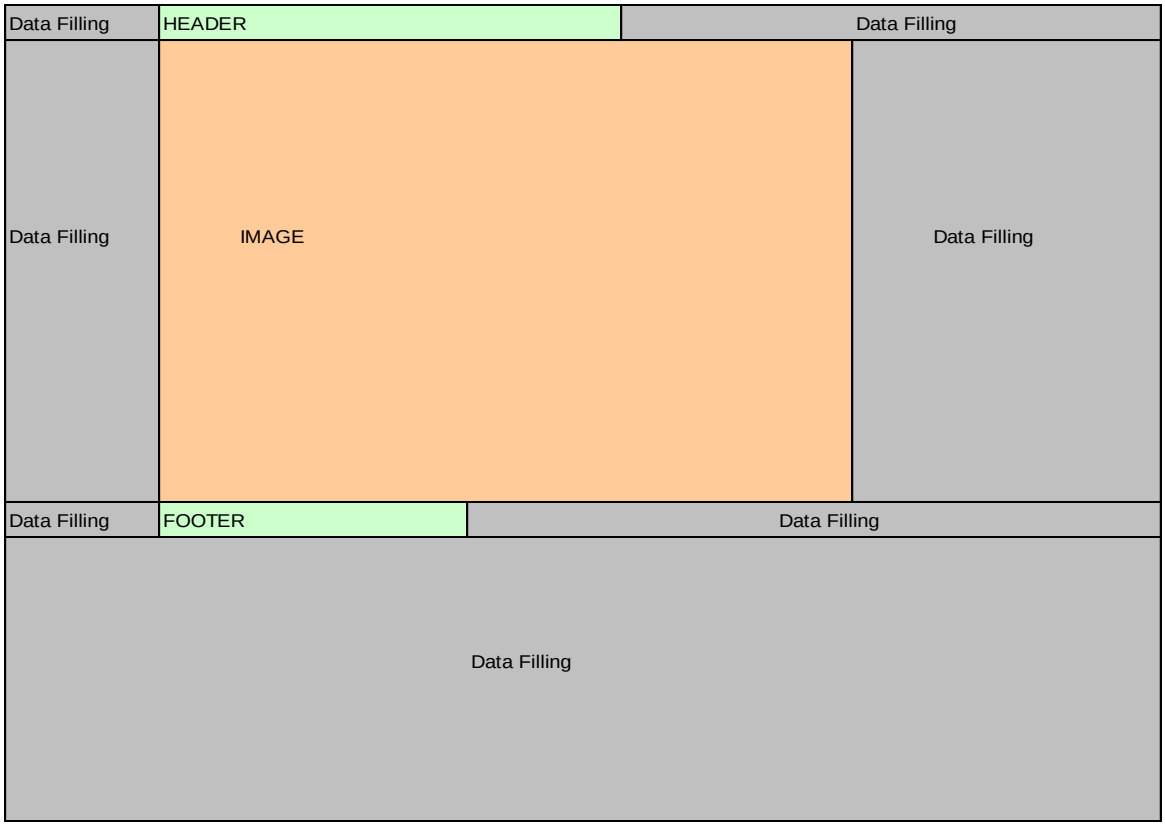
- 6 LVDS pairs for pixel data
- 1 LVDS pair for synchronization
- 1 LVDS pair for pixel clock

Figure 9 : LVDS pairs organization



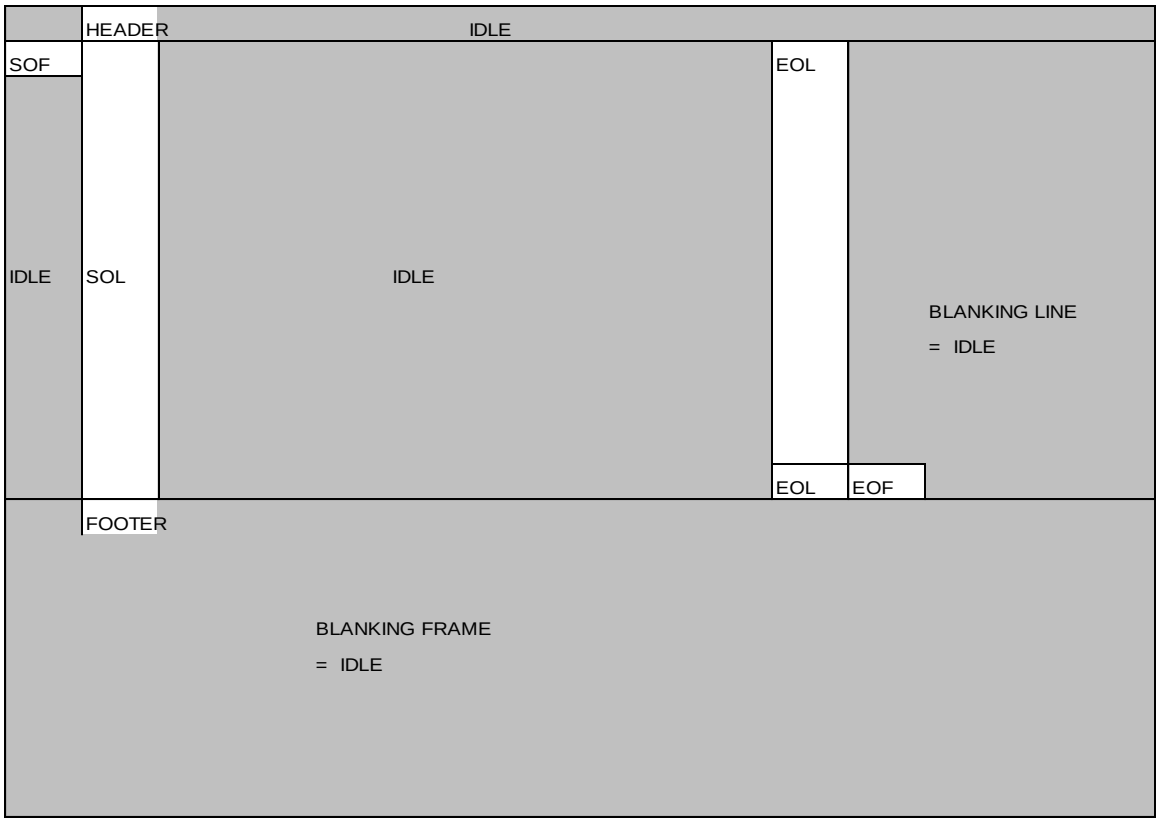
The Data and Synchronization Channel are organized as described below.

Figure 10 : LVDS Data organization



Note: Data filling can be changed using dedicated SPI register.

Figure 11 : LVDS Synchronization signal



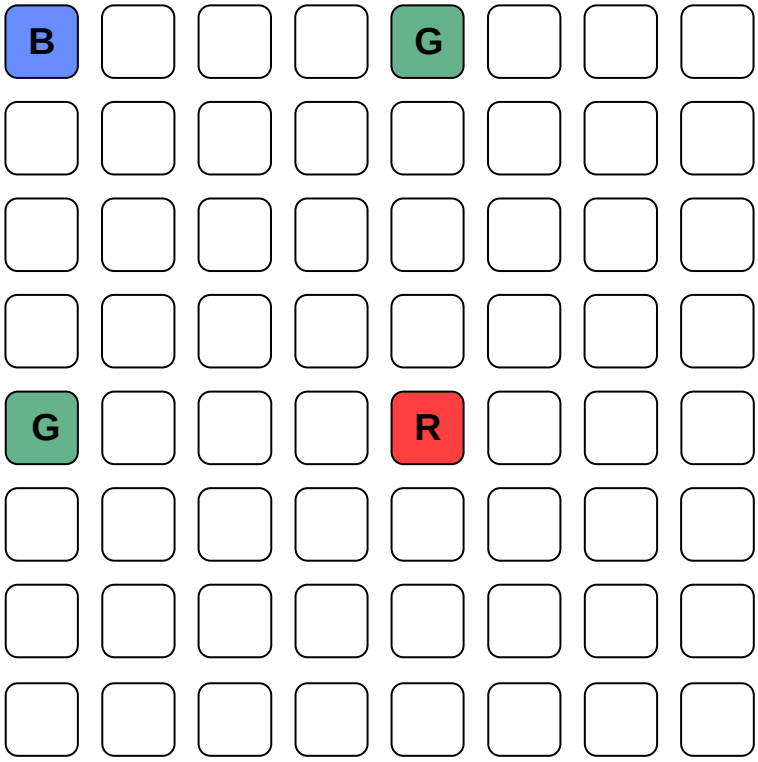
8.2 Serial Peripheral Interface

The EV76C664 contains internal registers used for the sensor operation. These registers can be programmed using the Serial Peripheral Interface (SPI).

9. SENSOR OPTIONS

The EV76C664 sensor is available in two versions:

- Monochrome,
- Sparse color filter array (pattern described below).



10. STANDARDS COMPLIANCE

The EV76C664 sensor conforms to the following standards:

- RoHS compliant
- Product qualification according to JEDEC JESD47

11. ORDERING CODES

11.1 Standard version with protective foil

- EV76C664ABT-RTR Monochrome product,
- EV76C664AMT-RTR Sparse product.

The EV76C664 is not supposed to be soldered

For other packaging or Color Filter Arrangement (CFA), please contact e2v.
The sensors are delivered in Jedec trays of 40 units each.

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