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LS4K
High speed CMOS System on Chip line scan image sensor

4k, 7µm Pixel, 18klps & 2k, 14µm Pixel, 33klps Line Scan CMOS Sensor

KEY BENEFITS

- High speed CMOS System on Chip (SoC) with dual pixel array
  - 7µm active pixel resolution: 2 rows x 4,096 pixels
  - 14µm active pixel resolution: 4 rows x 2,048 pixels
- Electronic global shutter with programmable exposition time
- Maximum line rate
  - 18,180lps at 4k resolution
  - 32,870lps at 2k resolution
- 65dB dynamic range (DR)
- SNRmax
  - 45dB (7µm pixel)
  - 48dB (14µm pixel)
- 0dB to 30dB programmable gain in 1dB steps
- Pixel binning for increased SNR
- Line windowing and sub-sampling with faster line rate
- On chip PRNU, DSNU, and lens shading correction
- 700mW maximum power consumption

TYPICAL APPLICATIONS

- Printed circuit board inspection
- High performance document scanning
- Flat panel display inspection
- General machine vision & food sorting
- OCT, medical

SENSOR OVERVIEW

The LS4k is a high speed CMOS System on Chip (SoC) line scan image sensor optimized for applications requiring short exposure times and high accuracy line rates. It incorporates on chip two pixel arrays consisting of 2 rows with 4,096 7µm pitch pixels and 4 rows with 2,048 14µm pitch pixels respectively, a high accuracy (12-bit) high speed (84MHz) analog-to-digital conversion (ADC), and sophisticated on chip optical calibration for PRNU, DSNU, and lens shading correction.

The line sensor array utilizes active CMOS pixels with pinned photodiodes to deliver high image quality whilst maintaining size, cost, and integration advantages of the CMOS process. The readout path permits pixel binning, increasing response and line rate. Windowing or sub-sampling allows a maximum line rate of 82,400 lines per second (lps) for 512-pixel window to be achieved.

The line rate, image sub-sampling, windowing, binning, exposure time, gain, and other image processing features are controlled via the sensor configuration registers. The LS4k incorporates an SPI port to communicate with an external host device and three high speed LVDS ports for data output. The reference voltages are generated on chip from an internal band gap reference. No external components are required and a power down mode is available for low current consumption when the device is inactive.

SENSOR CHARACTERISTICS	
Optical format – mm	35
Active imager size – mm	28.672
Active pixel	2 rows x 4,096 4 rows x 2,048
Pixel size	7µm active pixel resolution: 2 rows x 4,096 pixels 14µm active pixel resolution: 4 rows x 2,048 pixels
Pixel type	4T with pinned photodiode
Shutter type	Electronic global shutter
Frame rate – lps	18,180 at 4k resolution 32,870 at 2k resolution 54,850 at 1k resolution 82,400 at 0.5k resolution
Sensing modes	PWC, pre-programmed trigger, continuous
Dynamic range – dB	65
SNRmax – dB	45 (7µm pixel) 48 (14µm pixel) 53.5 (14µm pixel, 4 rows binning)

PRNU – %	0.65
DSNU – %	0.03
QE (@550nm)	61% 14µm pixel 93% 7µm pixel
Pixel response	157 DN (nJ/cm^2) for 7µm pixel 197 DN (nJ/cm^2) for 14µm pixel

MISCELLANEOUS	
Power supply – V	Dual 3.3/1.8
Maximum power consumption – mW	700
Operating junction temperature – °C	-30 to +70
Packages	40 pin dual in-line ceramic